Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A scramble control method for a switching system, said switching system comprising:

a switch having input ports and output ports, said switch operative for switchably interconnecting said input ports with said output ports;

a plurality of input interfaces each connected to a corresponding input port of the switch, each of the input interfaces including a scrambler, each scrambler having a pseudorandom pattern generator, wherein each of the input interfaces inputs data to sequentially output frames including scrambled data to the corresponding input port of the switch; and

a plurality of output interfaces each connected to a corresponding output port of the switch, each of the output interfaces including a descrambler, each descrambler having a pseudorandom pattern generator, wherein each of the output interfaces inputs frames including scrambled data from the corresponding output port of the switch to output frames of original data, and wherein each of the pseudorandom pattern generators of the scramblers and the descramblers generates a same pseudorandom pattern when initialized with a same input value,

said scramble control method comprising the steps of:

resetting the scramblers simultaneously to initialize the pseudorandom pattern generators of the scramblers with the same input value, so as to synchronize the scramblers;

resetting the descramblers simultaneously to initialize the pseudorandom pattern generators of the descramblers with the same input value, so as to synchronize the descramblers and to establish synchronization between the scramblers and the descramblers; and

continuously maintaining synchronization between the scramblers and the descramblers when the switch performs a switching operation~~;~~

wherein the scramblers are simultaneously initialized at a first time point and thereafter are not reset;

wherein the descramblers are simultaneously initialized at a second time point and thereafter are not reset; and

wherein the second time point is delayed from the first time point by a time period required for transferring a frame from an input interface to an appropriate output interface through the switch.

2. (Cancelled)

3. (Currently Amended) The scramble control method according to claim ~~2~~ 1, wherein the first time point is a time when the switching system starts up.

4. (Original) The scramble control method according to claim 1, wherein the scramblers and descramblers are of frame synchronizing type.

5. (Previously Presented) The scramble control method according to claim 4, wherein a cycle of the pseudorandom patterns generated by the pseudorandom pattern generators of the scramblers and the descramblers is set to be longer than a length of the frame.

6. (Previously Presented) The scramble control method according to claim 5, wherein the pseudorandom pattern generators of the scramblers and the descramblers use a generator polynomial specified by: $1 + X^{43}$.

7. – 15. (Cancelled)

16. (Currently Amended) A switching system comprising:

a switch having input ports and output ports, said switch operative for switchably interconnecting said input ports with said output ports;

a plurality of input interfaces each connected to a corresponding input port of the switch, each of the input interfaces including a scrambler, each scrambler having a pseudorandom pattern generator, wherein each of the input interfaces inputs data to

sequentially output frames including scrambled data to the corresponding input port of the switch;

a plurality of output interfaces each connected to a corresponding output port of the switch, each of the output interfaces including a descrambler, each descrambler having a pseudorandom pattern generator, wherein each of the output interfaces inputs frames including scrambled data from the corresponding output port of the switch to output frames of original data; and

a reset pulse generator for generating a scrambler reset pulse and a descrambler reset pulse, wherein the scrambler reset pulse is sent to all the scramblers at equal timing, and the descrambler reset pulse is sent to all the descramblers at equal timing;

wherein each of the pseudorandom pattern generators of the scramblers and the descramblers generates a same pseudorandom pattern when initialized with a same input value;

wherein the pseudorandom pattern generators of the scramblers are initialized to the same input value when the scramblers receive the scrambler reset pulse, so as to synchronize the scramblers;

wherein the pseudorandom pattern generators of the descramblers are initialized to the same input value when the descramblers receive the descrambler reset pulse, so as to synchronize the descramblers and to establish synchronization between the scramblers and the descramblers; ~~and~~

wherein synchronization between the scramblers and the descramblers is continuously maintained when the switch performs a switching operation~~.~~;

wherein the scramblers are initialized in response to the scrambler reset pulse and thereafter are not reset;

wherein the descramblers are initialized in response to the descrambler reset pulse and thereafter are not reset; and

wherein the descrambler reset pulse is delayed from the scrambler reset pulse by a time period required for transferring a frame from an input interface to an appropriate output interface through the switch.

17. – 21. (Cancelled)